

**IN74HC4094**

**8-Bit Serial-Input Shift Register  
With Latched 3-State Outputs  
High-Performance Silicon-Gate CMOS**

The IN74HC4094 is identical in pinout to the LS/ALS4094. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

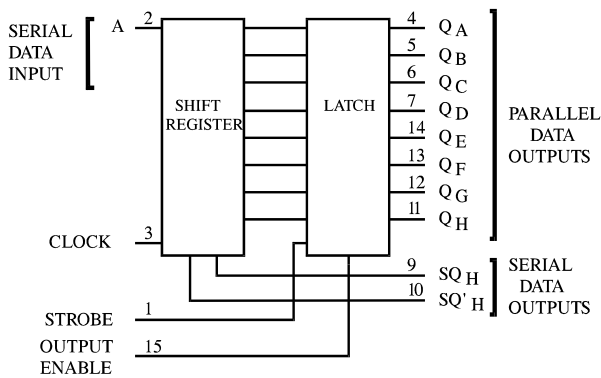
This device consists of an 8-bit shift register and 8-bit D-type latch with three-state parallel outputs. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage SQ<sub>H</sub> can be used to cascade several devices.

Data on the SQ<sub>H</sub> output is transferred to a second output (SQ<sub>H</sub>') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch, which latches data on the negative going transition of the Strobe input signal. When the Strobe input is held high, data propagates through the latch to a 3-state output buffer.

This buffer is enabled when Output Enable input is taken high.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

**LOGIC DIAGRAM**



PIN 16 = V<sub>CC</sub>  
PIN 8 = GND

N SUFFIX PLASTIC  
D SUFFIX SOIC

**ORDERING INFORMATION**  
IN74HC4094N Plastic  
IN74HC4094D SOIC  
T<sub>A</sub> = -55° to 125° C for all packages

**PIN ASSIGNMENT**

STROBE	1	16	V <sub>CC</sub>
A	2	15	OUTPUT ENABLE
CLOCK	3	14	Q <sub>E</sub>
Q <sub>A</sub>	4	13	Q <sub>F</sub>
Q <sub>B</sub>	5	12	Q <sub>G</sub>
Q <sub>C</sub>	6	11	Q <sub>H</sub>
Q <sub>D</sub>	7	10	SQ <sub>H</sub>
GND	8	9	SQ <sub>H</sub> '

**FUNCTION TABLE**

Inputs				Parallel Outputs		Serial Outputs	
Clock	Output Enable	Strobe	A	Q <sub>A</sub>	Q <sub>N</sub>	SQ <sub>H</sub>	SQ <sub>H</sub> '
	L	X	X	Z	Z	Q <sub>6</sub>	NC
	L	X	X	Z	Z	NC	SQ <sub>H</sub>
	H	L	X	NC	NC	Q <sub>6</sub>	NC
	H	H	L	L	Q <sub>N-1</sub>	Q <sub>6</sub>	NC
	H	H	H	H	Q <sub>N-1</sub>	Q <sub>6</sub>	NC
	H	X	X	NC	NC	NC	SQ <sub>H</sub>

NC = No Change  
Z = high impedance  
X = don't care

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package +	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			
	V <sub>CC</sub> = 2.0 V	0	1000	ns
	V <sub>CC</sub> = 4.5 V	0	500	
	V <sub>CC</sub> = 6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0	4.0	40	160	μA

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0	6	5	4	MHz
		4.5	30	25	20	
		6.0	35	28	23	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to SQ <sub>H</sub> (Figures 1 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q <sub>A</sub> -Q <sub>H</sub> (Figures 2 and 5)	2.0	195	245	295	ns
		4.5	40	50	60	
		6.0	33	42	50	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay ,Output Enable to Q <sub>A</sub> -Q <sub>H</sub> (Figures 3 and 6)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay ,Output Enable to Q <sub>A</sub> -Q <sub>H</sub> (Figures 3 and 6)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
C <sub>IN</sub>	Maximum Input Capacitance	-	10	10	10	pF
C <sub>OUT</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q <sub>A</sub> -Q <sub>H</sub>	-	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)	Typical @25°C, V <sub>CC</sub> =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D = C_{PD}V_{CC}^2f + I_{CC}V_{CC}$	300			

**TIMING REQUIREMENTS**( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>su</sub>	Minimum Setup Time, Serial Data Input A to Clock (Figure 4)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9.0	11	13	
t <sub>h</sub>	Minimum Hold Time, Clock to Data Input A (Figure 4)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t <sub>w</sub>	Minimum Pulse Width, Strobe (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

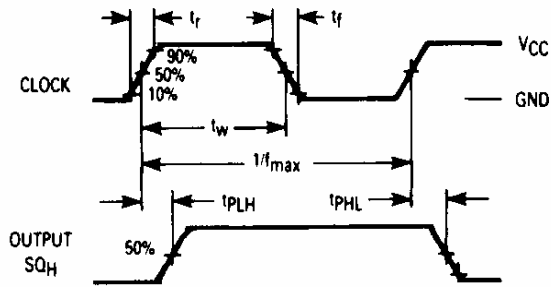


Figure 1. Switching Waveforms

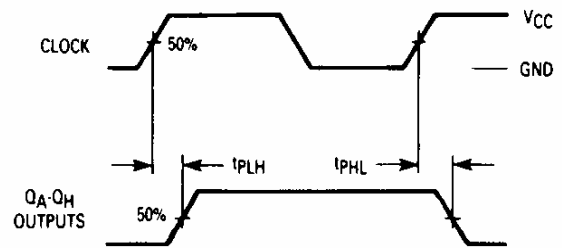


Figure 2. Switching Waveforms

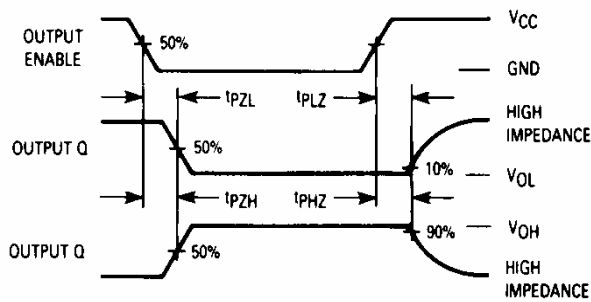


Figure 3. Switching Waveforms

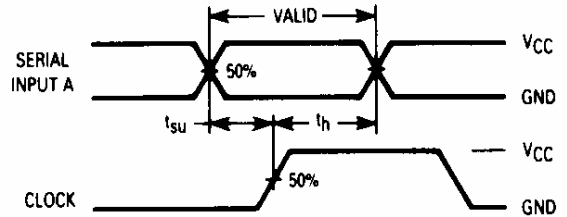
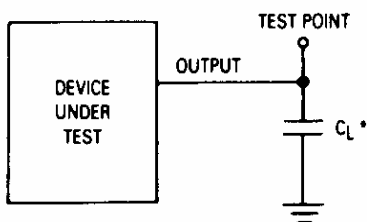
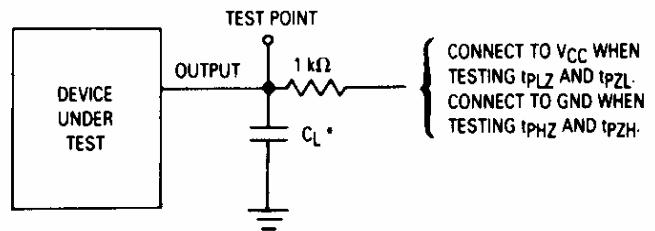


Figure 4. Switching Waveforms



\*Includes all probe and jig capacitance.

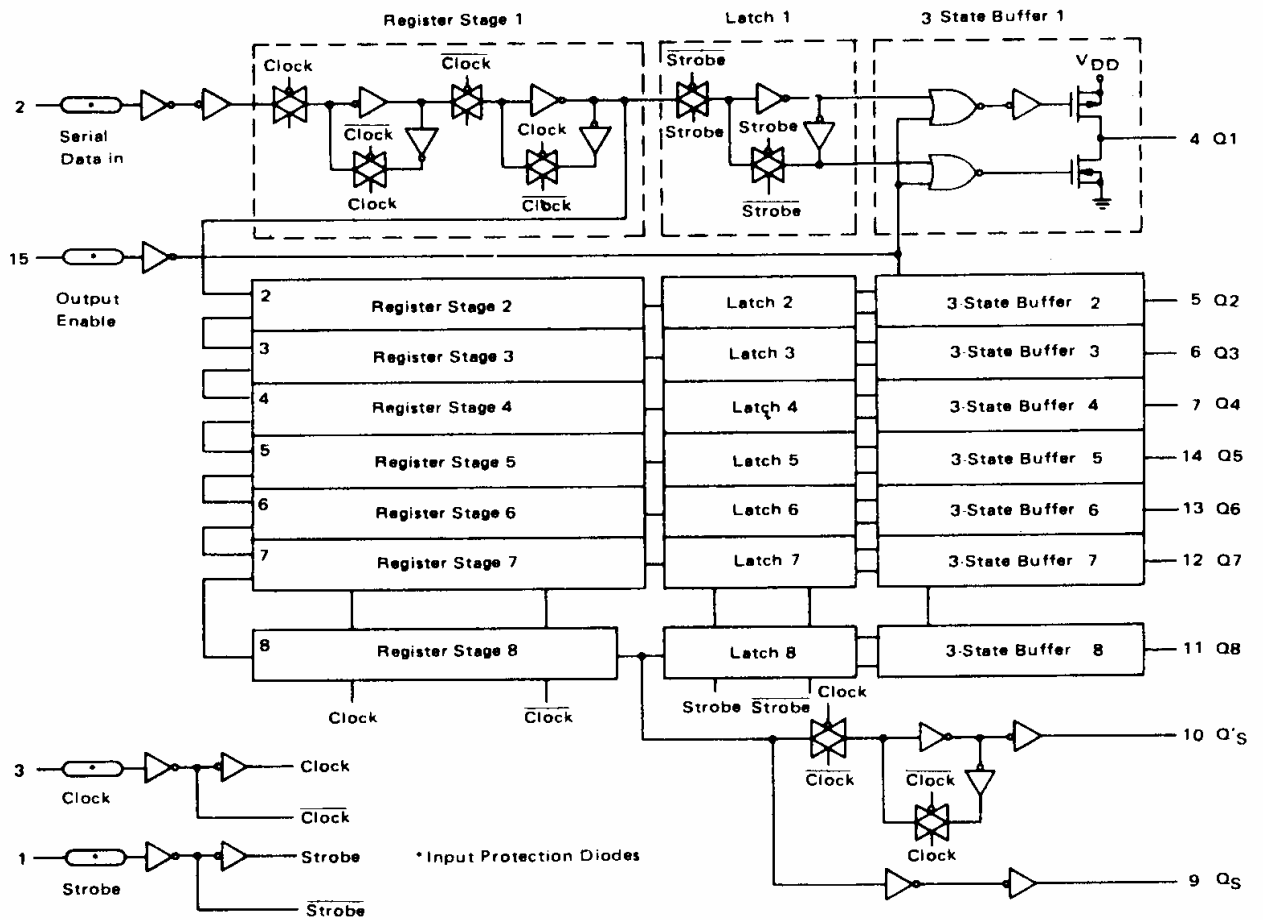
Figure 5. Test Circuit



\*Includes all probe and jig capacitance.

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



## TIMING DIAGRAM

