

VOLTAGE RISE CONVERTERS FAMILY

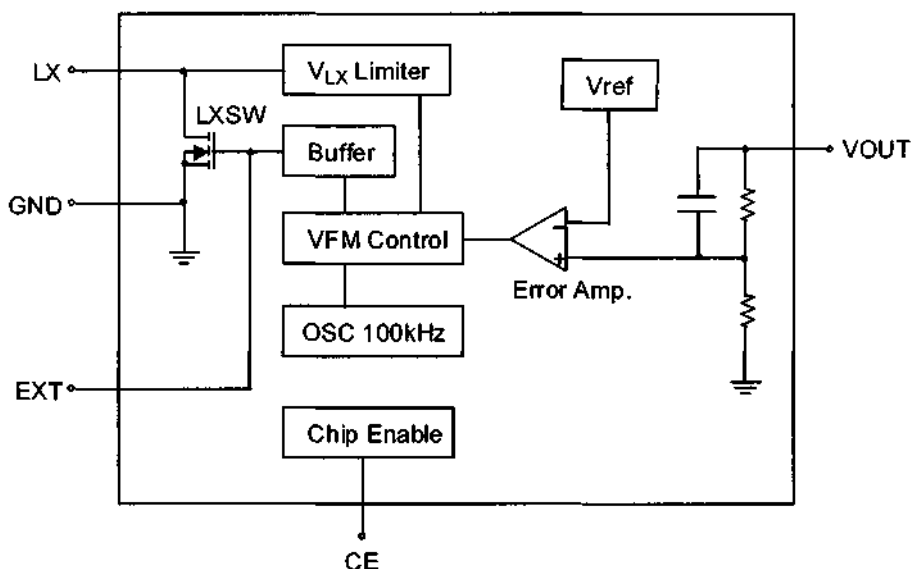
General Description

The IZ9261-15, IZ9261-25, IZ9261-33, IZ9261-50 are VFM Step-up DC/DC ICs (pulse voltage regulators with output voltages 1.5; 2.5; 3.3; 5.0V. The ICs of pulse voltage regulators are purposed for use in power supply sources of consumer & industrial electronic devices with battery-power sourcing. The application of this ICs permit to keep constant output voltage of power supply source even in the case of low charge level of the battery.

Features

- Minimal Number of External Components (Only an inductor, a diode, and a capacitor)
- Low Input Current (5 μ A at Switch Off State)
- High Output Voltage Accuracy \pm 2%
- Low Ripple and Low Noise
- Low Start-up Voltage, 0.85V at 1mA
- 75% Efficiency with Low Cost Inductor
- Low Temperature-Drift +50 ppm/ $^{\circ}$ C

Block diagram



Pad Description

Pad Number	Symbol	Pad Function
01	CE	Chip Enable Input
02	UOUT	Output
03	LX	Switching
04	EXT	External control
05-15	-	Technological pad (used for fusion)
04	GND	Ground (Common)

Maximum Ratings & Recommended operation conditions

Parameter, unit	Unit	Recommended operation conditions		Maximum Ratings	
		Min.	Max.	Min.	Max.
Output Voltage, V	U_{OUT}	-	$U_{OUT} \pm 2\%^*$	-	8
LX Pin Voltage, V	U_{LX}	-	7	-	8
EXT Pin Voltage, V	U_{EXT}	0.4	$U_{OUT} - 0.4$	-0.3	$U_{OUT} + 0.3$ B
CE Pin Voltage, V	U_{CE}	0	U_{OUT}	-0.3	$U_{OUT} + 0.3$ B
LX Pin Output Current, mA	I_{LX}	-	10	-	250
EXT Pin Current, I_{EXT}				-50	50

* $U_{OUT} = 1.5\text{ V} \pm 2\%$ for IZ9261-15,
 $U_{OUT} = 2.5\text{ V} \pm 2\%$ for IZ9261-25,
 $U_{OUT} = 3.3\text{ V} \pm 2\%$ for IZ9261-33,
 $U_{OUT} = 5\text{ V} \pm 2\%$ for IZ9261-50.

Conversion efficiency ratio ($T_a = 25\text{ }^\circ\text{C}$)

Parameter, Unit		Symbol	Mode of measurement	Typical value
Conversion efficiency ratio, %	IZ9261-15,	η	$U_{IN} = 1.4\text{ V}$	75
	IZ9261-25, IZ9261-33		$U_{IN} = 1.8\text{ V}$	75
	IZ9261-50		$U_{IN} = 3\text{ V}$	85

Electrical features
(For application without external input transistor)

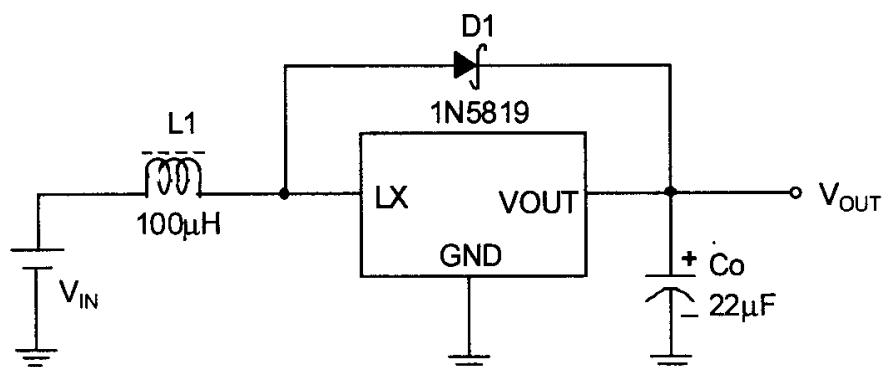
Parameter, unit		Symbol	Test Conditions	Norm		T _A , °C
				Min	Max	
Output Voltage Accuracy, %		ΔU_{OUT}		-2	+2	25±10
				-3	+3	-25...+85
Start-up Voltage, V		U_{ST}	$I_{OUT} = 1 \text{ mA};$ $U_{IN} : 0 \rightarrow 2 \text{ V}$	-	1.0	25±10
					1.2	-25...+85
Hold-on Voltage, V		U_{HO}	$I_{OUT} = 1 \text{ mA};$ $U_{IN} : 2 \rightarrow 0 \text{ V}$	-	0.7	25±10
					0.8	-25...+85
Input Current 1, μA	IZ9261-15,	I_{IN1}	$U_{IN} = 1.4 \text{ V};$ $U_{SS} = 0 \text{ V}$	-	18	25±10
	IZ9261-25, IZ9261-33		$U_{IN} = 1.8 \text{ V};$ $U_{SS} = 0 \text{ V}$	-	18	
	IZ9261-50		$U_{IN} = 3 \text{ V};$ $U_{SS} = 0 \text{ V}$	-	24	
Input Current 2, μA	IZ9261-15,	I_{IN2}	$U_{OUT} = U_{OUT} + 0.5 \text{ V};$ $U_I = 1.4 \text{ V};$	-	8	25±10
					12	-25...+85
	IZ9261-25, IZ9261-33		$U_{OUT} = U_{OUT} + 0.5 \text{ V};$ $U_I = 1.8 \text{ V};$	-	8	25±10
					12	-25...+85
	IZ9261-50		$U_{OUT} = U_{OUT} + 0.5 \text{ V}$ $U_I = 3 \text{ V}$	-	10	25±10
					15	-25...+85
LX Switching Current, mA	IZ9261-15, IZ9261-25, IZ9261-33	$I_{SWITCHING}$	$U_{LX} = 0.4 \text{ V}$	60	-	25±10
				40		-25...+85
	IZ9261-50		$U_{LX} = 0.4 \text{ V}$	80	-	25±10
				55		-25...+85
LX Leakage Current, μA		$I_{LEAKAGE}$	$U_{LX} = 6 \text{ V}$	-	0.5	25±10
					1.0	-25...+85
CE High level voltage, V	IZ9261-15,	U_{CE-H}	$U_{IN} = U_{OUT} \times 0.9$	0.8	-	-25...+85
	IZ9261-25, IZ9261-33			0.4 × U_{OUT}	-	25±10
				IZ9261-50	0.6 × U_{OUT}	-
CE Low level voltage, V		U_{CE-L}	$U_{IN} = U_{OUT} \times 0.9$	-	0.2	25±10
					0.15	-25...+85
Input Current for High Level on CE pin, μA		$I_{IN-CE-H}$	CE = U_{OUT}	-	0.5	25±10
					1.0	-25...+85
Input Current for Low Level on CE pin, μA		$I_{IN-CE-L}$	CE = 0 V	-0.5	-	25±10
				-1.0		-25...+85
Maximum Oscillator Frequency, kHz		F_{MAX}		80	160	25±10
				40	200	-25...+85
Oscillator Duty Cycle, %		D_{OSC}	Low Level on LX pin	65	85	25±10
				55	85	-25...+85
Voltage Limit, V		U_{LX}	LX switched on	0.65	1.0	25±10

Electrical features

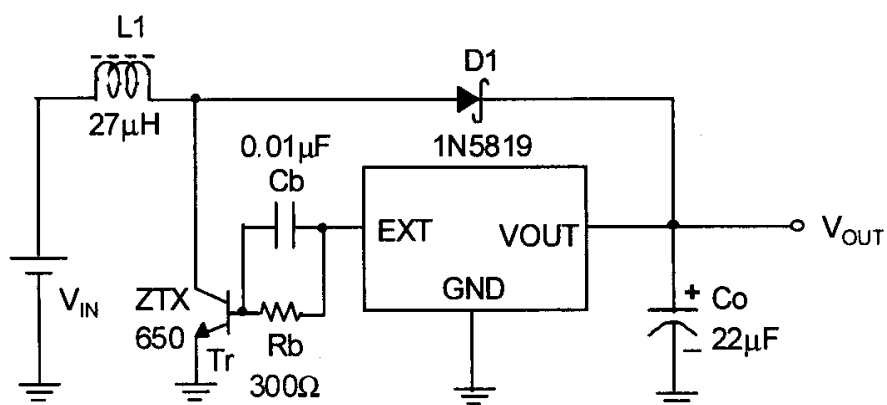
 (T_A = 25 °C, For application with external input transistor)

Parameter, unit	Symbol	Test Conditions	Norm		T _A , °C		
			Min	Max			
Output Voltage Accuracy, %	ΔU_{OUT}		-2	+2	25±10		
			-3	+3	-25...+85		
Start-up Voltage, V	U _{ST}	I _{OUT} = 1 mA; U _{IN} : 0→2 V	-	1.0	25±10		
				1.2	-25...+85		
Hold-on Voltage, V	U _{HO}	I _{OUT} = 1 mA; U _{IN} : 2→0 V	-	0.7	25±10		
				0.8	-25...+85		
Input Current 1, μA	I _{IN1}	U _{IN} = 1.4 V;	-	50	25±10		
			I _{IN1}	U _{IN} = 1.8 V;		-	50
						I _{IN1}	U _{IN} = 3 V;
Input Current 2, μA	I _{IN2}	U _{OUT} = U _{OUT} +0.5V; U _I = 1.4 V;	-	10	25±10		
			I _{IN2}	U _{OUT} = U _{OUT} +0.5V; U _I = 1.8 V;	-	15	-25...+85
	I _{IN2}	U _{OUT} =U _{OUT} +0.5V U _I = 3 V			-	10	25±10
			I _{IN2}	U _{OUT} =U _{OUT} +0.5V U _I = 3 V	-	15	-25...+85
	I _{IN2}	U _{OUT} =U _{OUT} +0.5V U _I = 3 V			-	10	25±10
			I _{IN2}	U _{OUT} =U _{OUT} +0.5V U _I = 3 V	-	15	-25...+85
Output Current for Low Level on EXT pin, mA	I _{O-EXT-H}	U _{EXT} = U _{OUT} -0.4 V I _{OUT} =10mA			-1.5	-	25±10
			-2.0	-	-		
Output Current for Low Level on EXT pin, mA	I _{O-EXT-L}	U _{EXT} = 0.4 V	1.5	-	25±10		
			1.0	-	-25...+85		
			2.0	-	25±10		
			1.5	-	-25...+85		
LX Leakage Current, μA	I _{LEAKAGE}	U _{LX} = 6 V	-	0.5	25±10		
				1.0	-25...+85		
CE High level voltage, V	U _{CE-H}	U _{IN} = U _{OUT} × 0.9	0.8	-	-25...+85		
			0.4 × U _{OUT}	-	25±10		
			0.6 × U _{OUT}	-	-25...+85		
CE Low level voltage, V	U _{CE-L}	U _{IN} = U _{OUT} × 0,9	-	0.2	25±10		
				0.15	-25...+85		
Input Current for High Level on CE pin, μA	I _{IN-CE-H}	CE = U _{OUT}	-	0.5	25±10		
				1.0	-25...+85		
Input Current for Low Level on CE pin, μA	I _{IN-CE-L}	CE = 0 V	-0.5	-	25±10		
			-1.0	-	-25...+85		
Maximum Oscillator Frequency, kHz	F _{MAX}		80	160	25±10		
			40	200	-25...+85		
Oscillator Duty Cycle, %	D _{OSC}	Low Level on LX pin	65	85	25±10		
			55	85	-25...+85		
Voltage Limit, V	U _{LX}	LX switched on	0.65	1.0	25±10		

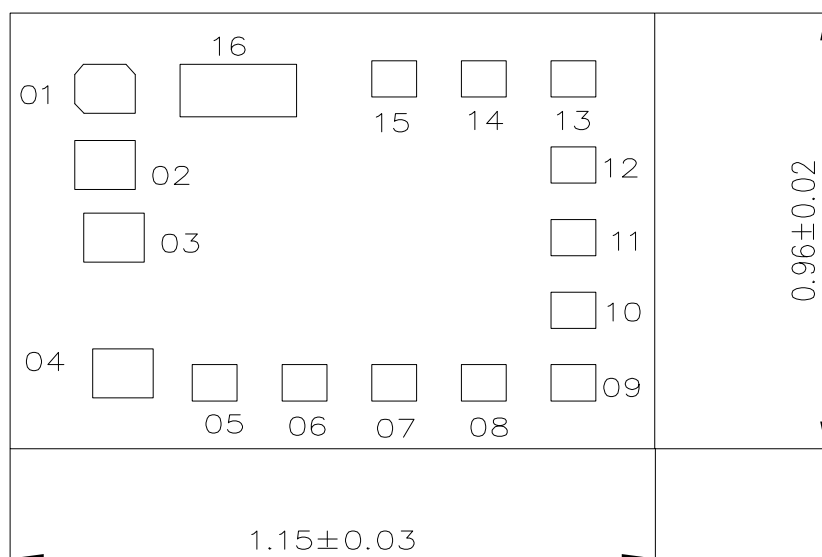
Application diagram without external input transistor



Application diagram with external input transistor



Die drawing



PAD LOCATION TABLE

Pad number	Coordinates (left bottom corner), mm		Contact pad size, mm (by passivation layer)
	X	Y	
01	0.116	0.747	0.108 x 0.108
02	0.116	0.579	0.108 x 0.108
03	0.132	0.419	0.108 x 0.108
04	0.148	0.120	0.108 x 0.108
05	0.337	0.109	0.080 x 0.080
06	0.497	0.109	0.080 x 0.080
07	0.657	0.109	0.080 x 0.080
08	0.817	0.109	0.080 x 0.080
09	0.977	0.109	0.080 x 0.080
10	0.977	0.269	0.080 x 0.080
11	0.977	0.429	0.080 x 0.080
12	0.977	0.589	0.080 x 0.080
13	0.977	0.779	0.080 x 0.080
14	0.817	0.779	0.080 x 0.080
15	0.657	0.779	0.080 x 0.080
16	0.329	0.739	0.208 x 0.116