

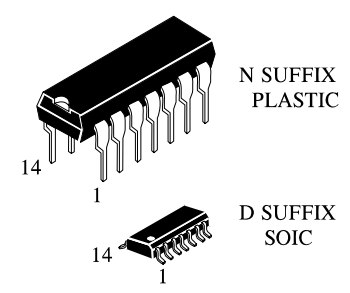
IN74LV04

Hex Inverter

The IN74LV04 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT04A.

The IN74LV04 provides six inverting buffers.

- Wide Operating Voltage: 1.0÷5.5 V
- Optimized for Low Voltage applications: 1.0÷3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Low Input Current

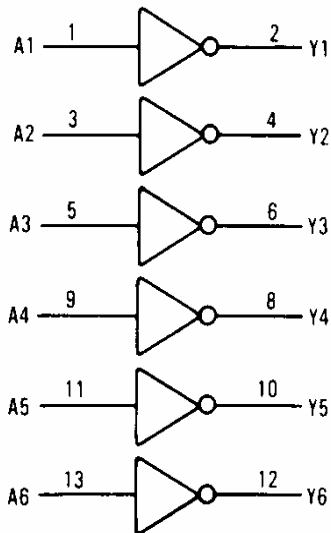


ORDERING INFORMATION

IN74LV04N	Plastic
IN74LV04D	SOIC
IZ74LV04	Chip

$T_A = -40^\circ \div 125^\circ$ C for all packages

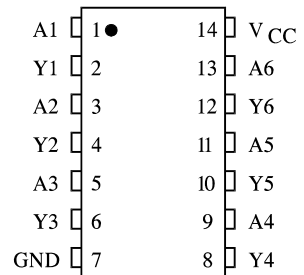
LOGIC DIAGRAM



$Y = \bar{A}$

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC supply voltage (Referenced to GND)	-0.5 ÷ +7.0	V
I _{IK} * ¹	DC input diode current	±20	mA
I _{OK} * ²	DC output diode current	±50	mA
I _O * ³	DC output source or sink current -bus driver outputs	±25	mA
I _{GND}	DC GND current for types with - bus driver outputs	±50	mA
I _{CC}	DC V _{CC} current for types with - bus driver outputs	±50	mA
P _D	Power dissipation per package, plastic DIP+ SOIC package+	750 500	mW
T _{stg}	Storage temperature	-65 ÷ +150	°C
T _L	Lead temperature, 1.5 mm from Case for 10 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C

SOIC Package: : - 8 mW/°C from 70° to 125°C

*¹: V_I < -0.5V or V_I > V_{CC}+0.5V

*²: V_O < -0.5V or V_O > V_{CC}+0.5V

*³: -0.5V < V_O < V_{CC}+0.5V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	1.0	5.5	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-40	+125	°C
t _r , t _f	Input Rise and Fall Time			
	V _{CC} = 1.2 V	0	1000	ns
	V _{CC} = 2.0 V	0	700	
	V _{CC} = 3.0 V	0	500	
	V _{CC} = 3.6 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} , V	Guaranteed Limit						Unit
				25°C		-40°C ÷ 85°C		-40°C ÷ 125°C		
				min	max	min	max	min	max	
V _{IH}	High-Level Input Voltage		1.2	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	
			3.0	2.1	-	2.1	-	2.1	-	
			3.6	2.5	-	2.5	-	2.5	-	
V _{IL}	Low-Level Input Voltage		1.2	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	
			3.0	-	0.9	-	0.9	-	0.9	
			3.6	-	1.1	-	1.1	-	1.1	
V _{OH}	High-Level Output Voltage	V _I = V _{IL} I _O = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V
		2.0	1.92	-	1.9	-	1.9	-	-	
			*	2.92	-	2.9	-	2.9	-	
		V _I = V _{IL} I _O = -6.0 μA	*	2.48	-	2.34	-	2.20	-	V
V _{OL}	Low-Level Output Voltage	V _I = V _{IH} I _O = 50 μA	1.2	-	0.09	-	0.1	-	0.1	V
			2.0	-	0.09	-	0.1	-	0.1	
				V _I = V _{IH} or V _{IL} I _O = 6.0 mA	3.0	-	0.33	-	0.4	-
I _{IL}	Low-Level Input Leakage Current			-	-0.1	-	-1.0	-	-1.0	μA
I _{IH}	High-Level Input Leakage Current	V _I = V _{CC}	*	-	0.1	-	1.0	-	1.0	μA
I _{CC}	Quiescent Supply Current (per Package)	V _I = 0 B or V _{CC} I _O = 0 μA	*	-	2.0	-	20	-	40	μA

* : V_{CC} = (3.3 ± 0.3) V

AC ELECTRICAL CHARACTERISTICS ($C_L=50$ pF, $t_{LH} = t_{HL} = 6.0$ ns, $V_{IL}=0V$, $V_{IH}=V_{CC}$, $R_L=1$ k Ω)

Symbol	Parameter	V _{CC} V	Guaranteed Limit						Unit
			25°C		-40°C ÷ 85°C		-40°C ÷ 125°C		
			min	max	min	max	min	max	
t _{THL} , (t _{TLH})	Output Transition Time, Any Output (Figure 1)	1.2	-	70	-	85	-	100	ns
		2.0	-	16	-	20	-	24	
		*	-	10	-	13	-	15	
t _{PHL} , (t _{PLH})	Propagation Delay, Input A to Output Y (Figure 1)	1.2	-	90	-	120	-	150	
		2.0	-	23	-	28	-	34	
		*	-	14	-	18	-	21	
C _I	Input Capacitance	3.0	-	-	-	3.5	-	3.5	pF

C _{PD}	Power Dissipation Capacitance (Per Inverter)	T _A =25°C, V _I =0V÷V _{CC}	pF
		42	

Used to determine the no-load dynamic power consumption:

$$P_D = C_{PD}V_{CC}^2f_I + \sum(C_LV_{CC}^2fo), f_I - \text{input frequency, } fo - \text{output frequency (MHz)}$$

$\sum(C_LV_{CC}^2fo)$ – sum of the outputs

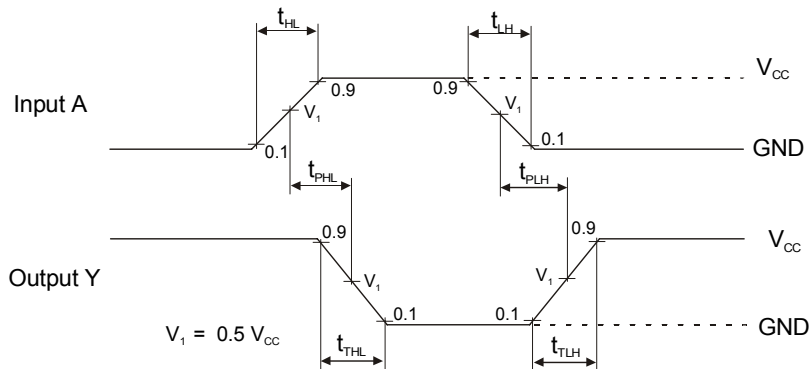


Figure 1. Switching Waveforms

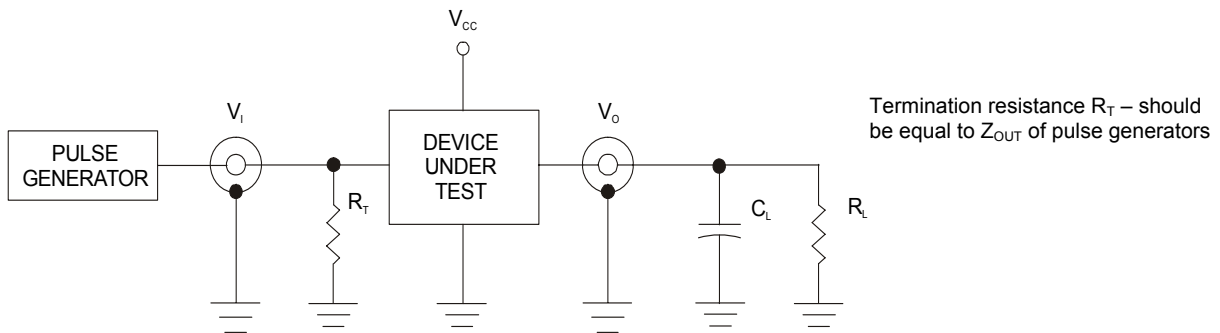
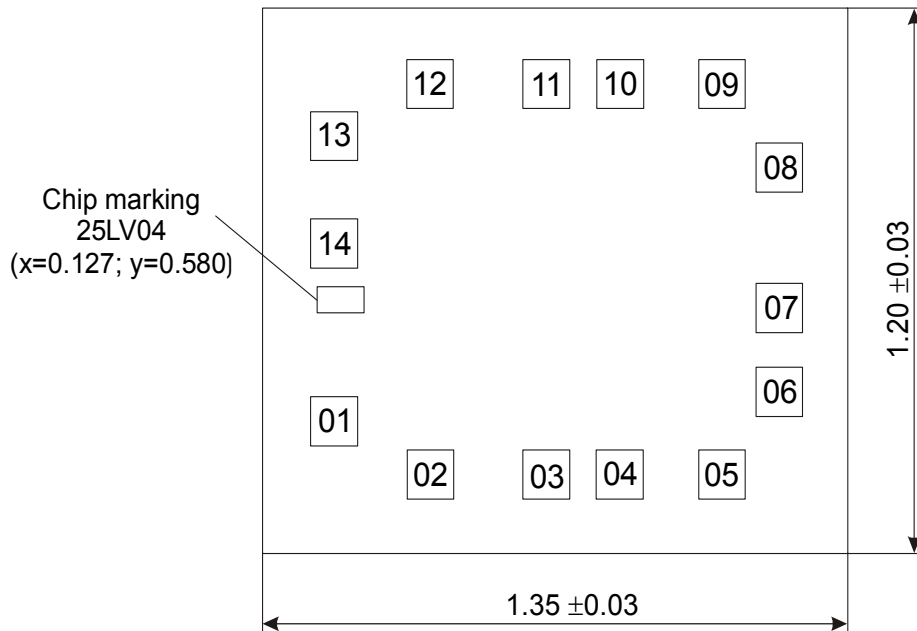


Figure 2. Test Circuit

CHIP PAD DIAGRAM IZ74LV04



Pad size 0.108 x 0.108 mm (Pad size is given as per metallization layer)

Thickness of chip 0.46 ± 0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	A1	0.111	0.228
02	Y1	0.333	0.111
03	A2	0.600	0.111
04	Y2	0.770	0.111
05	A3	1.006	0.111
06	Y3	1.138	0.293
07	GND	1.138	0.477
08	Y4	1.138	0.786
09	A4	1.006	0.970
10	Y5	0.771	0.970
11	A5	0.600	0.970
12	Y6	0.332	0.970
13	A6	0.111	0.855
14	Vcc	0.111	0.619