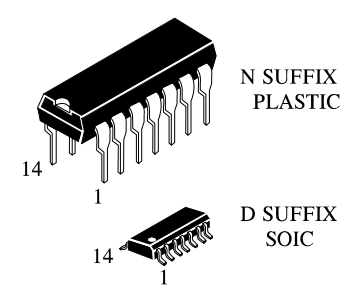


**IN74HC21A**

**Dual 4-Input AND Gate**

The IN74HC21A is high-speed Si-gate CMOS device and is pin compatible with pullup resistors with low power Schottky TTL (LSTTL). The device provide the Dual 4-input AND function.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices

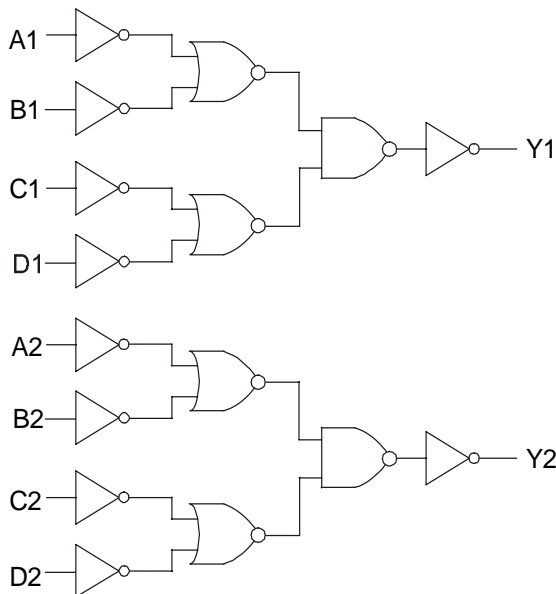


**ORDERING INFORMATION**

IN74HC21AN	Plastic
IN74HC21AD	SOIC
IZ74HC21A	Chip

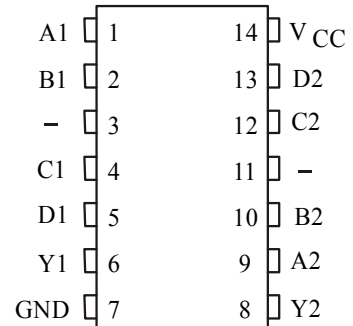
$T_A = -55^\circ$  to  $125^\circ$  C for all packages

**LOGIC DIAGRAM**



PIN 14 =  $V_{CC}$   
PIN 7 = GND

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs				Output
A	B	C	D	Y
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

X = don't care

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

\*\*Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			ns
	V <sub>CC</sub> =2.0 V	0	1000	
	V <sub>CC</sub> =4.5 V	0	500	
	V <sub>CC</sub> =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

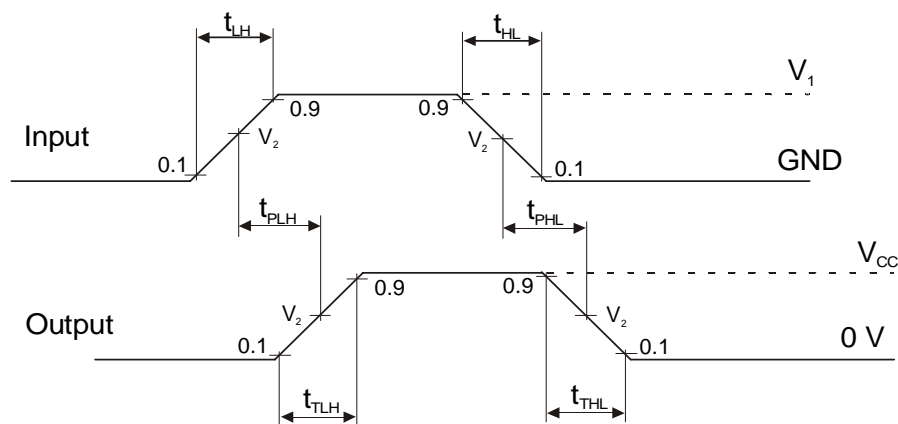
**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit	
				25 °C to -55°C	≤85 °C	≤125 °C		
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0	1.5	1.5	1.5	V	
			3.0	2.1	2.1	2.1		
			4.5	3.15	3.15	3.15		
			6.0	4.2	4.2	4.2		
V <sub>IL</sub>	Maximum Low -Level Input Voltage		2.0	0.5	0.5	0.5	V	
			3.0	0.9	0.9	0.9		
			4.5	1.35	1.35	1.35		
			6.0	1.8	1.8	1.8		
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   = -50 μA	2.0	1.92	1.9	1.9	V	
			3.0	2.92	2.9	2.9		
			4.5	4.42	4.4	4.4		
			6.0	5.92	5.9	5.9		
			V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   = -2.4 mA	3.0	2.48	2.34		2.2
			V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   = -4 mA	4.5	3.98	3.84		3.7
			V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   = -5.2 mA	6.0	5.48	5.34		5.2
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   = 50 μA	2.0	0.09	0.1	0.1	V	
			3.0	0.09	0.1	0.1		
			4.5	0.09	0.1	0.1		
			6.0	0.09	0.1	0.1		
			V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   = 2.4 mA	3.0	0.26	0.33		0.4
			V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   = 4 mA	4.5	0.26	0.33		0.4
			V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   = 5.2 mA	6.0	0.26	0.33		0.4
I <sub>IL</sub>	Maximum Low-Level Input Leakage Current	V <sub>IN</sub> = 0 V	6.0	-0.1	-1.0	-1.0	μA	
I <sub>IH</sub>	Maximum High-Level Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub>	6.0	0.1	1.0	1.0	μA	
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> =V <sub>CC</sub> or 0 V	6.0	4.0	40	160	μA	

AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

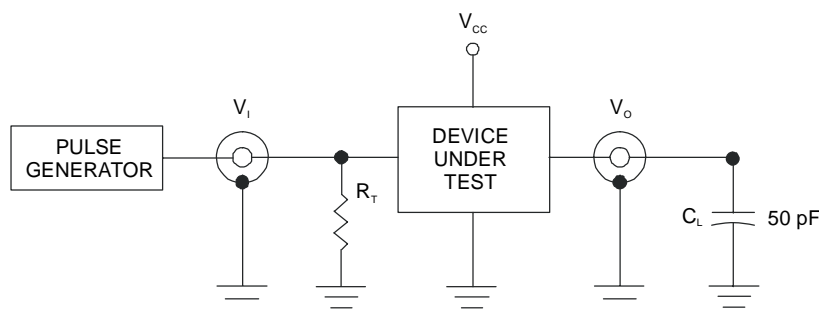
Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay (Figure 1)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Transition Time (Figure 1)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>IN</sub>	Maximum Input Capacitance	5.0	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate)	T <sub>A</sub> =25°C, V <sub>CC</sub> =5.0 V			pF
	Used to determine the no-load dynamic power consumption: P <sub>D</sub> =C <sub>PD</sub> V <sub>CC</sub> <sup>2</sup> f+I <sub>CC</sub> V <sub>CC</sub>	50			



$$V_1 = 0.5 V_{CC}$$

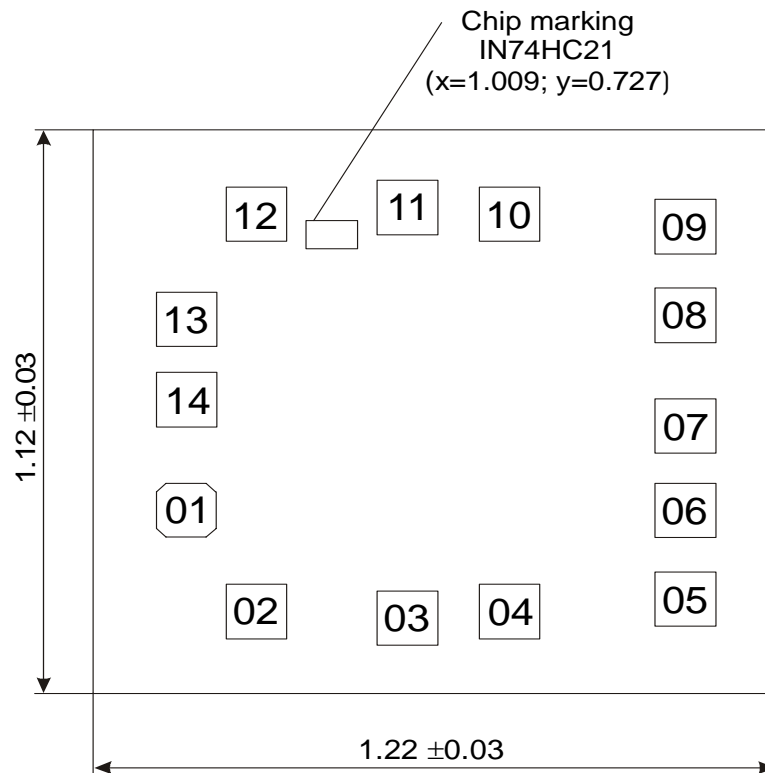
Figure 1. Switching Waveforms



Termination resistance  $R_T$  – should be equal to  $Z_{OUT}$  of pulse generators

Figure 2. Test Circuit

CHIP PAD DIAGRAM IZ74HC21A



Pad size 0.108 x 0.108 mm (Pad size is given as per passivation layer)  
Thickness of chip 0.46 ± 0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	A1	1.1165	0.3160
02	B1	0.2405	0.1150
03	-	0.5105	0.1020
04	C1	0.6925	0.1150
05	D1	1.0065	0.1400
06	Y1	1.0065	0.3160
07	GND	1.0065	0.4840
08	Y2	1.0065	0.7040
09	A2	1.0065	0.8800
10	B2	0.6925	0.9050
11	-	0.5105	0.9180
12	C2	0.2405	0.9050
13	D2	0.1165	0.6960
14	Vcc	0.1165	0.5360