

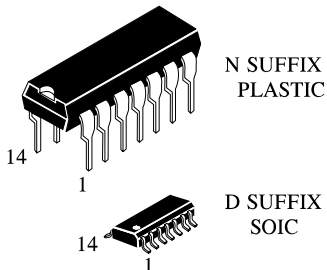
**IN74HC125A**

**Quad 3-State Noninverting Buffers**

The IN74HC125A is identical in pinout to the LS/ALS125. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The IN74HC125A noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX  
PLASTIC

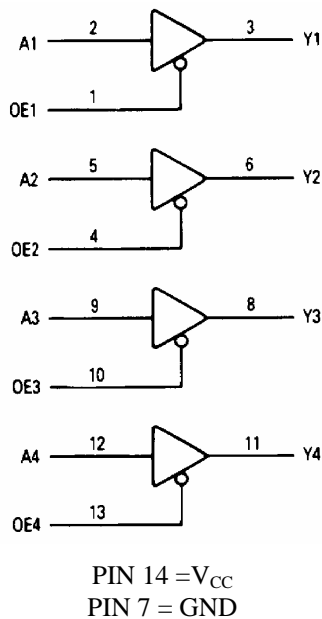
D SUFFIX  
SOIC

**ORDERING INFORMATION**

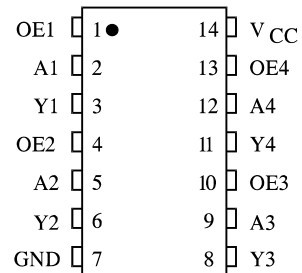
IN74HC125AN Plastic  
IN74HC125AD SOIC  
IZ74HC125 Chip

$T_A = -55^\circ$  to  $125^\circ$  C for all packages

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs		Output
A	OE	Y
H	L	H
L	L	L
X	H	Z

X = don't care  
Z = high impedance

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)			
	V <sub>CC</sub> =2.0 V	0	1000	ns
	V <sub>CC</sub> =4.5 V	0	500	
	V <sub>CC</sub> =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> =0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V <sub>IN</sub> =V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V <sub>IN</sub> =V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	4.0	40	160	μA

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0	90	115	135	ns
		4.5	18	23	27	
		6.0	15	20	23	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0	90	115	135	ns
		4.5	18	23	27	
		6.0	15	20	23	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>IN</sub>	Maximum Input Capacitance	-	10	10	10	pF
C <sub>OUT</sub>	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Buffer)	Typical @25°C, V <sub>CC</sub> =5.0 V		pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	45		

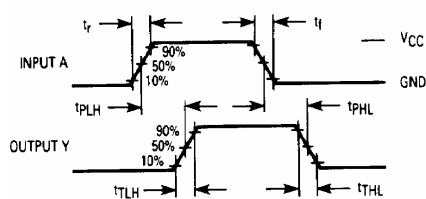


Figure 1. Switching Waveforms

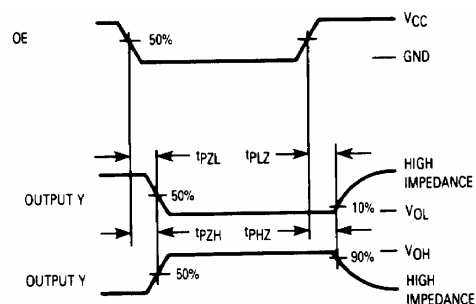
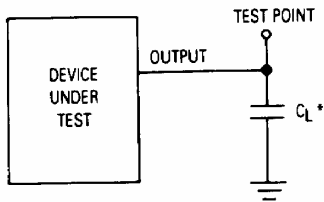
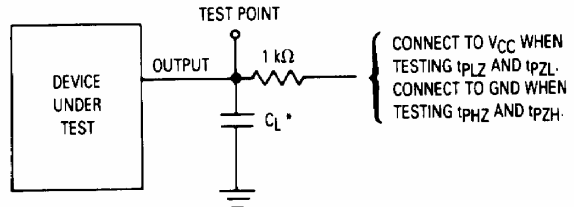


Figure 2. Switching Waveforms



\*Includes all probe and jig capacitance.

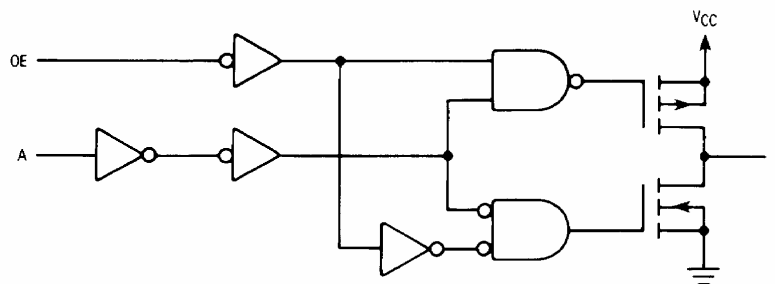
Figure 3. Test Circuit



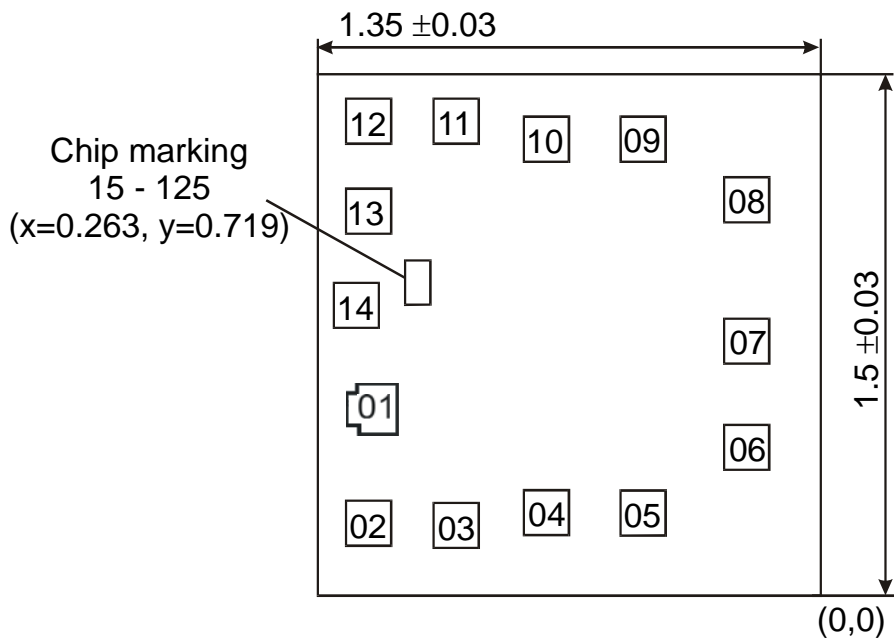
\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

**EXPANDED LOGIC DIAGRAM**  
(1/4 of the Device)



CHIP PAD DIAGRAM IZ74HC125



Pad size 0.106 x 0.106 mm (Pad size is given as per passivation layer)

Thickness of chip 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	OE1	0.169	0.49
02	A1	0.169	0.122
03	Y1	0.464	0.122
04	OE2	0.722	0.147
05	A2	1.031	0.147
06	Y2	1.124	0.408
07	GND	1.124	0.669
08	Y3	1.124	0.986
09	A3	1.031	1.247
10	OE3	0.722	1.247
11	Y4	0.464	1.272
12	A4	0.169	1.272
13	OE4	0.169	1.903
14	V <sub>CC</sub>	0.128	0.66