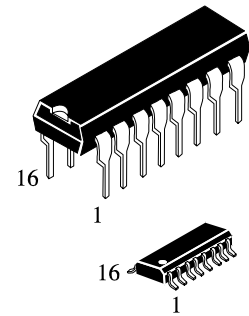


IW4015B

DUAL 4-STAGE STATIC SHIFT REGISTER

The IW4015B consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one IW4015B package, or to more than 8 stages using additional IW4015B's is possible.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 1.0 V min @ 5.0 V supply
 2.0 V min @ 10.0 V supply
 2.5 V min @ 15.0 V supply



N SUFFIX
PLASTIC

D SUFFIX
SOIC

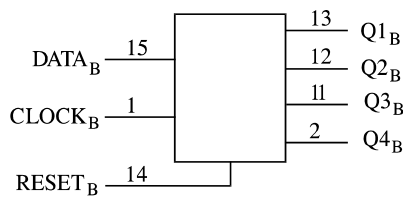
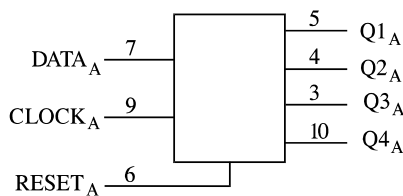
ORDERING INFORMATION

IW4015BN Plastic

IW4015BD SOIC

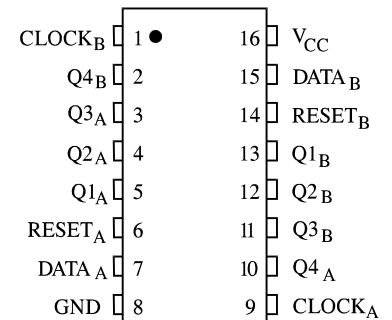
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 16=V_{CC}
PIN 8=GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Clock	Data	Reset	Q1	Q _n
	L	L	L	Q _{n-1}
	H	L	H	Q _{n-1}
	X	L	No change	
X	X	H	L	L

X = don't care

IW4015B

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to 20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} 0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} 0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P _D	Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

IW4015B

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5 V or V _{CC} - 0.5 V	5.0	3.5	3.5	3.5	V
		V _{OUT} =1.0 V or V _{CC} - 1.0 V	10	7	7	7	
		V _{OUT} =1.5 V or V _{CC} - 1.5 V	15	11	11	11	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.5 V or V _{CC} - 0.5 V	5.0	1.5	1.5	1.5	V
		V _{OUT} =1.0 V or V _{CC} - 1.0 V	10	3	3	3	
		V _{OUT} =1.5 V or V _{CC} - 1.5 V	15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.9	
		V _{IL} =1.5V, V _{IH} =3.5V, I _O =-1μA	5.0	4.5	4.5	5	
		V _{IL} =3.0V, V _{IH} =7.0V, I _O =-1μA	10	9.0	9.0	4.5	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
		V _{IL} =1.5V, V _{IH} =3.5V, I _O =1μA	5.0	0.5	0.5	0.5	
		V _{IL} =3.0V, V _{IH} =7.0V, I _O =1μA	10	1.0	1.0	1.0	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	1.0	1.0	30	μA
			10	2.0	2.0	60	
			15	4.0	4.0	120	
			20	20	20	600	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC}					mA
		V _{OL} =0.4 V	5.0	0.64	0.51	0.36	
		V _{OL} =0.5 V	10	1.6	1.3	0.9	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC}					mA
		V _{OH} =4.6 V	5.0	-0.64	-0.51	-0.36	
		V _{OH} =2.5 V	5.0	-2.0	-1.6	-	
		V _{OH} =9.5 V	10	-1.8	-1.3	1.15	
		V _{OH} =13.5 V	15	-4.2	-3.4	-0.9	
					-2.4		

IW4015B

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥ -55 $^{\circ}\text{C}$	25°C	≤ 125 $^{\circ}\text{C}$	
t_{max}	Maximum Clock Frequency (Figure 1)	5.0	3	3	1.5	MHz
		10	6	6	3	
		15	8.5	8.5	4.25	
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Clock to Q (Figure 1)	5.0	320	320	640	ns
		10	160	160	320	
		15	120	120	240	
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figure 2)	5.0	400	400	800	ns
		10	200	200	400	
		15	160	160	320	
t_{THL} , t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS ($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -$ 55°C	25°C	$\leq 125^{\circ}$ C	
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0	180	180	360	ns
		10	80	80	160	
		15	50	50	100	
t_w	Minimum Pulse Width, Reset (Figure 2)	5.0	200	200	400	ns
		10	80	80	160	
		15	60	60	120	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	5.0	70	70	140	ns
		10	40	40	80	
		15	30	30	60	
t_h	Minimum Hold Time, Clock to Data (Figure 3)	5.0	0	0	0	ns
		10	0	0	0	
		15	0	0	0	
t_r , t_f	Maximum Input Rise and Fall Time (Figure 1)	5.0	15	15	30	μs
		10	6	6	12	
		15	2	2	4	

IW4015B

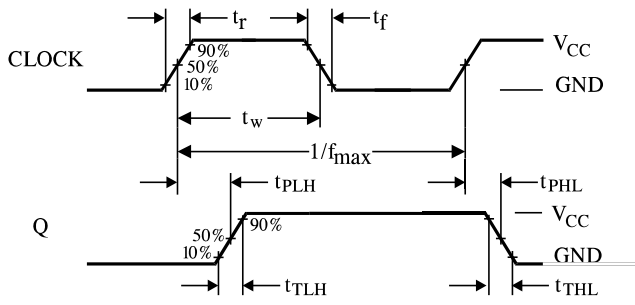


Figure 1. Switching Waveforms

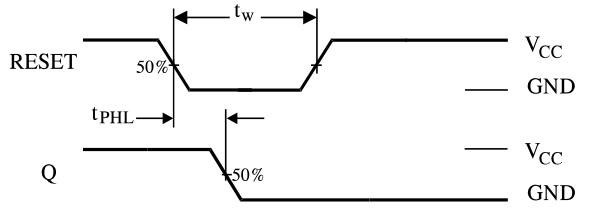


Figure 2. Switching Waveforms

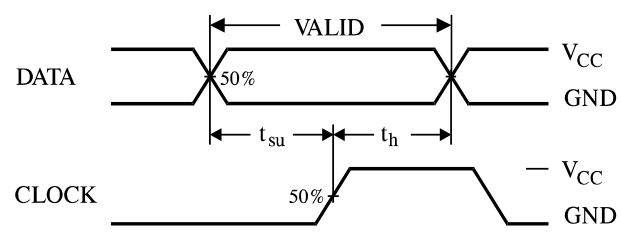
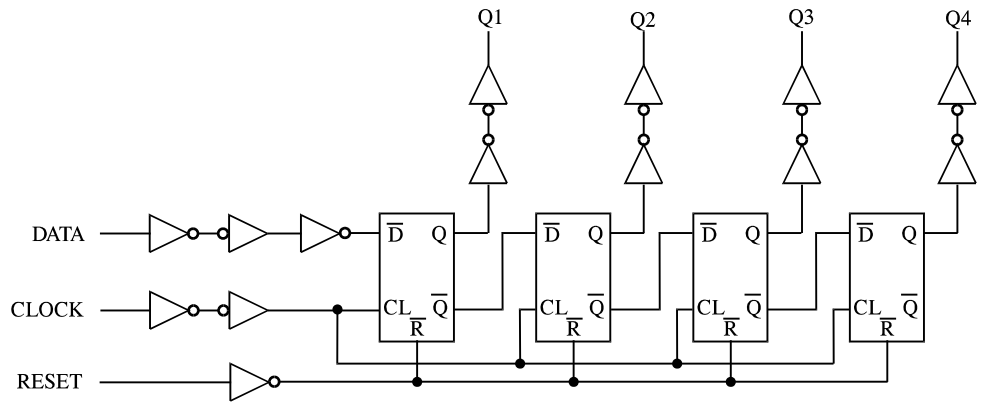


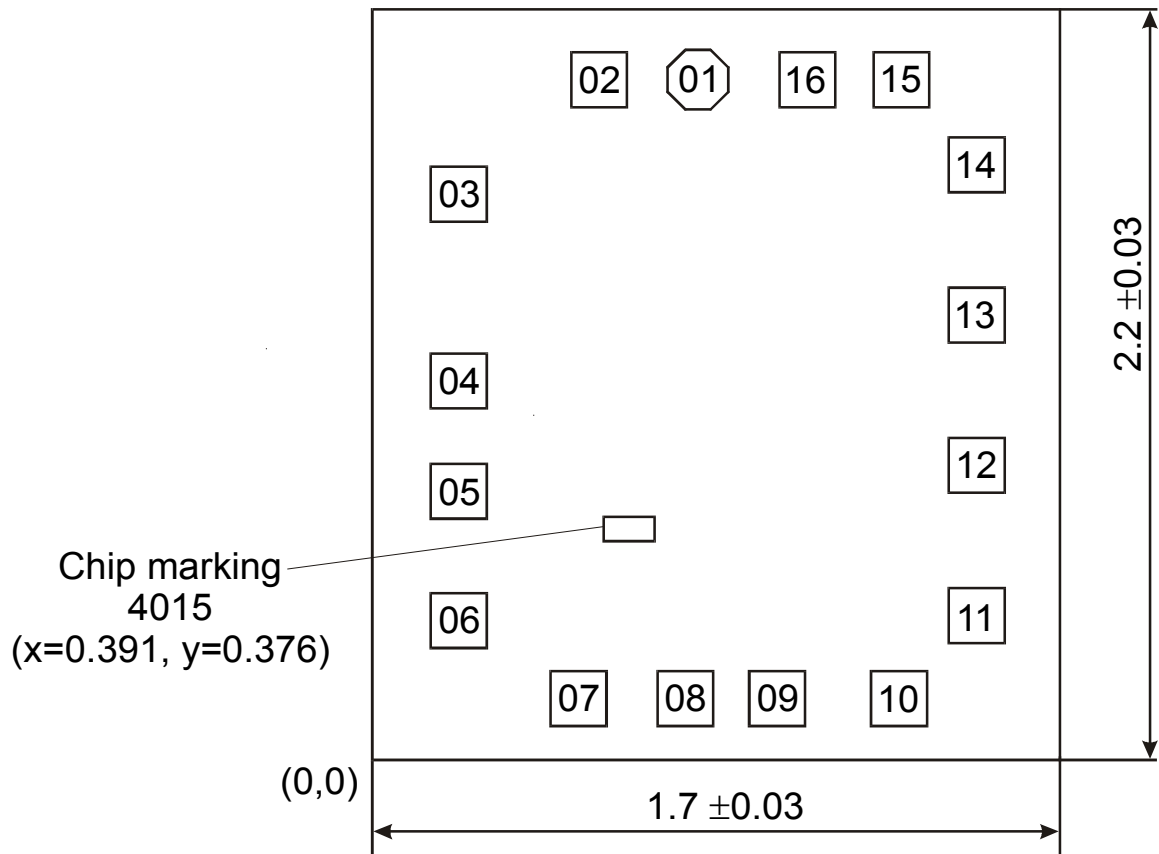
Figure 3. Switching Waveforms

EXPANDED LOGIC DIAGRAM (1/2 of the Device)



IW4015B

CHIP PAD DIAGRAM IZ4015B



Pad size 120 x 120 μm (Pad size is given as per metallization layer)
Thickness of chip 0.46 ± 0.02 mm

PAD LOCATION

Pad №	Symbol	X	Y
01	CLOCK _B	0.907	1.980
02	Q4 _B	0.493	1.980
03	Q3 _A	0.121	1.796
04	Q2 _A	0.121	1.217
05	Q1 _A	0.121	0.714
06	RESET _A	0.121	0.295
07	DATA _A	0.188	0.121
08	GND	0.455	0.121
09	CLOCK _A	0.666	0.121
10	Q4 _A	1.085	0.121
11	Q3 _B	1.450	0.304
12	Q2 _B	1.450	0.882
13	Q1 _B	1.450	1.385
14	RESET _B	1.450	1.805
15	DATA _B	1.385	1.980
16	V _{cc}	1.117	1.980